WHAT IS CLAIMED IS:

1. A processing core comprising:

R-number processing pipelines each comprising N-number of processing paths, wherein each of said R-number of processing pipelines are synchronized to operate as a single very long instruction word (VLIW) processing core, said VLIW processing core being configured to process R x N-number of VLIW sub-instructions in parallel.

2. The processing core as recited in claim 1 wherein said R-number of processing pipelines can be configured to operate independently as separately operating pipelines.

3. The processing core as recited in claim 1 wherein each of said R-number of processing pipelines comprises S-number of register files, such that said processing core comprises R x S-number of register files.

4. The processing core as recited in claim 3 wherein each of said R-number of processing pipelines comprises one register file for every two of said N-number of processing paths, such that S = N/2.

5. The processing core as recited in claim 3 wherein each of said register files comprises Q-number of M-bit wide registers, and wherein said Q-number of registers within each of said register files are either private or global registers, and wherein when a value is written to one of said Q-number of said registers which is a global register within one of said register files, said value is propagated to a corresponding global register in the other of said register files, and wherein when a value is written to one of said Q-number of said registers which is a private register within one of said register files, said value is not propagated to a corresponding register in the other of said register files.

6. The processing core as recited in claim 1, wherein a single VLIW processing instruction comprises R x N-number of P-bit sub-instructions appended together.

7. The processor chip as recited in claim 6, wherein M=64, Q=64, and P=32.

8. The processing core as recited in claim 3 wherein said each of said R-number of processing pipelines comprise an execute stage which includes an execute unit for

each of said N-number processing paths, each of said execute units comprising an integer processing unit, a load/store processing unit, a floating point processing unit, or any combination of one or more of said integer processing units, said load/store processing units, and said floating point processing units.

9. The processing core as recited in claim 8 wherein an integer processing unit and a floating point processing unit share one of said register files.

10. The processing core as recited in claim 5 wherein Q=64, and a 64-bit special register stores bits indicating whether registers in the register files are private registers or global registers, each bit in the 64-bit special register corresponding to one of the registers in the register files.

11. The processing core as recited in claim 5 wherein a plurality of said register files are connected to a bus, and a value written to a global register in one of said register files connected to the bus is propagated to a corresponding global register in the other of said register files connected to across bus across said bus.

12. The processing core as recited in claim 5 wherein a plurality of said register files are connected together in serial, and a value written to a first global register in a first of said plurality of register files is propagated to a corresponding first global register in a second of said plurality of register files connected directly to said first of said plurality of register files.

13. In a computer system, a scalable computer processing architecture, comprising:

one or more processor chips, each comprising:

a processing core, including:

R-number processing pipelines each comprising N-number of processing paths, wherein each of said R-number of processing pipelines are synchronized to operate as a single very long instruction word (VLIW) processing core, said VLIW processing core being configured to process R x N-number of VLIW sub-instructions in parallel;

an I/O link configured to communicate with other of said one or more processor chips or with I/O devices;

a communication controller in electrical communication with said processing core and said I/O link;

said communication controller for controlling the exchange of data between a first one of said one or more processor chips and said other of said one or more processor chips;

wherein said computer processing architecture can be scaled larger by connecting together two or more of said processor chips in parallel via said I/O links of said processor chips, so as to create multiple processing core pipelines which share data therebetween.

14. The computer system as recited in claim 13 wherein said R-number of processing pipelines can be configured to operate independently as separately operating pipelines.

15. The computer system as recited in claim 13 wherein each of said R-number of processing pipelines comprises S-number of register files, such that said processing core comprises R x S-number of register files.

16. The computer system as recited in claim 15 wherein each of said R-number of processing pipelines comprises one register file for every two of said N-number of processing paths, such that S = N/2.

17. The computer system as recited in claim 15 wherein each of said register files comprises Q-number of M-bit wide registers, and wherein said Q-number of registers within each of said register files are either private or global registers, and wherein when a value is written to one of said Q-number of said registers which is a global register within one of said register files, said value is propagated to a corresponding global register in the other of said register files, and wherein when a value is written to one of said Q-number of said registers which is a private register within one of said register files, said value is not propagated to a corresponding register in the other of said register files.

18. The computer system as recited in claim 13 wherein a single VLIW processing instruction comprises R x N-number of P-bit sub-instructions appended together.

19. The computer system as recited in claim 18 wherein M=64, Q=64, and P=32.wherein M=64, Q=64, and P=32.

20. The computer system as recited in claim 15 wherein said each of said R-number of processing pipelines comprise an execute stage which includes an execute unit for each of said N-number processing paths, each of said execute units comprising an integer processing unit, a load/store processing unit, a floating point processing unit, or any combination of one or more of said integer processing units, said load/store processing units, and said floating point processing units.

21. The computer system as recited in claim 20 wherein an integer processing unit and a floating point processing unit share one of said register files.

22. The computer system as recited in claim 17 wherein Q=64, and a 64-bit special register stores bits indicating whether registers in the register files are private registers or global registers, each bit in the 64-bit special register corresponding to one of the registers in the register files.

23. The computer system as recited in claim 17 wherein a plurality of said register files are connected to a bus, and a value written to a global register in one of said register files connected to the bus is propagated to a corresponding global register in the other of said register files connected to across bus across said bus.

24. The computer system as recited in claim 17 wherein a plurality of said register files are connected together in serial, and a value written to a first global register in a first of said plurality of register files is propagated to a corresponding first global register in a second of said plurality of register files connected directly to said first of said plurality of register files.